IN THE CLAIMS

Amended claims follow:

1. (Previously Amended) An apparatus for processing data packets, comprising:

a first data processing unit adapted to filter incoming packets;

an addressable memory unit in which a plurality of instruction sets for packet processing are stored;

a second data processing unit adapted to process incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit; and

a data bus connecting the addressable memory unit and the first and second data processing units.

2. (Original) The apparatus of claim 1, further comprising a policy condition table connected to said first data processing unit, said policy condition table having a plurality of rules stored therein.

3. (Original) The apparatus of claim 1, further comprising a policy action table connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy.

4. (Original) The apparatus of claim 3, wherein at least one of said policies comprises:

a first address pointer element for identifying the location in said addressable memory unit of one of said plurality of instruction sets, and

a second address pointer element for identifying the location in said addressable memory unit of a state block.

5. (Original) The apparatus of claim 3, wherein said first data processing unit assigns a thread to each said incoming packet, wherein said thread corresponds to one of said policies stored in said policy action table.

6. (Original) The apparatus of claim 3, wherein said first data processing unit comprises logic for matching a first incoming packet to a stored first rule and for generating a first thread if the first incoming packet matches said first rule, said first thread identifying the location of one of said at least one data processing policies in said policy action table.

7. (Original) The apparatus of claim 6, wherein said second data processing unit is adapted to process the first incoming packet according to said data processing policy corresponding to said first thread.

8. (Original) The apparatus of claim 6, wherein said data processing policy comprises a first address pointer to a starting address of a first set of instructions and a second address pointer to a starting address of a state block stored in said addressable memory unit, said state block used by said first set of instructions for processing the first incoming packet.

9. (Original) The apparatus of claim 6, wherein said thread is assigned to said first incoming packet based on said first rule.

10. (Original) The apparatus of claim 6, wherein said first processing unit further comprises logic for matching a second incoming packet to a stored second rule and for generating a second thread if the second incoming packet matches the second rule, said second thread identifying the location of one of said at least one data processing policy in said policy action table.

11. (Original) The apparatus of claim 10, wherein said second data processing unit is adapted to process the second incoming packet according to said data processing policy corresponding to said second thread.

12. (Original) The apparatus of claim 10, wherein said second thread is assigned to said second incoming packet based on said second rule.

13. (Previously Amended) The apparatus of claim 3, wherein said first processing unit further comprises logic for matching a plurality of incoming packets to a stored corresponding plurality of rules and for generating a thread for each packet that matches one of said plurality of rules, each said thread identifying the location of one of said at least one data processing policy in said policy action table.

14. (Original) The apparatus of claim 13, wherein the second data processing unit is adapted to process each packet according to said data processing policy corresponding to said thread associated with said packet.

15. (Original) The apparatus of claim 13, further comprising a memory unit connected to said first data processing unit and to said second data processing unit, said memory unit adapted to temporarily store packets before processing by said second data processing unit.

16. (Original) The apparatus of claim 1, wherein said second data processing unit comprises a plurality of general purpose processors for executing instructions in parallel.

17. (Original) The apparatus of claim 16, wherein at least one said general purpose processor comprises a complex instruction set computer processor.

18. (Original) The apparatus of claim 16, wherein at least one said general purpose processor comprises a reduced instruction set computer processor.

19. - 29. (Cancelled)

30. (Previously Presented) An apparatus for processing data packets, comprising:

a first data processing unit adapted to filter incoming packets;

an addressable memory unit in which a plurality of instruction sets for packet processing are stored;

a second data processing unit adapted to process incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit; and

a data bus connecting the addressable memory unit and the first and second data processing units;

wherein a policy condition table is connected to said first data processing unit, said policy condition table having a plurality of rules stored therein;

wherein a policy action table is connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy;

wherein said first data processing unit comprises logic for matching a first incoming packet to a stored first rule and for generating a first thread if the first incoming packet matches said first rule, said first thread identifying the location of one of said at least one data processing policies in said policy action table;

wherein said second data processing unit is adapted to process the first incoming packet according to said data processing policy corresponding to said first thread;

wherein said data processing policy comprises a first address pointer to a starting address of a first set of instructions and a second address pointer to a starting address of a state block stored in said addressable memory unit, said

state block used by said first set of instructions for processing the first incoming packet;

wherein said first processing unit further comprises logic for matching a second incoming packet to a stored second rule and for generating a second thread if the second incoming packet matches the second rule, said second thread identifying the location of one of said at least one data processing policy in said policy action table;

wherein said second data processing unit is adapted to process the second incoming packet according to said data processing policy corresponding to said second thread;

wherein a memory unit is connected to said first data processing unit and to said second data processing unit, said memory unit adapted to temporarily store packets before processing by said second data processing unit;

wherein said second data processing unit comprises a plurality of general purpose processors for executing instructions in parallel;

wherein the apparatus includes a control logic unit coupled to an input and the policy condition table for feeding an arithmetic logic unit, which is in turn coupled to the policy action table and the state block for generating an output.